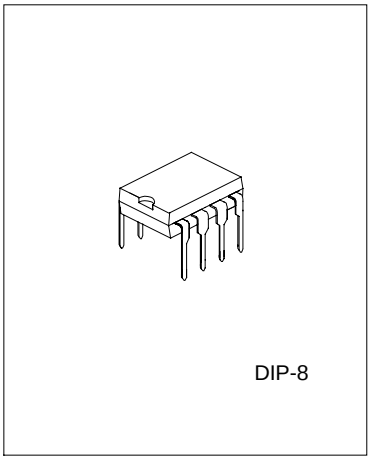
DTMF GENERATORS



DESCRIPTION

The SC9200A/B tone generators are designed for μC interfaces. They can be instructed by a μC to generate 16 dual tones and 8 single tones from the DTMF pin. The SC9200A provides a serial mode whereas the SC9200B contains a selectable serial/parallel mode interface for various applications such as security systems, home automation, remote control through telephone lines communication system, etc.

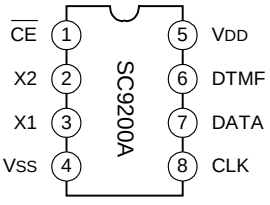
FEATURES

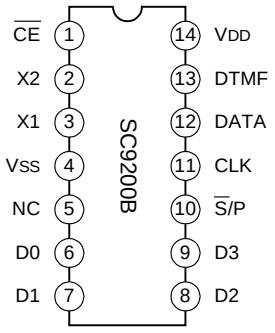
* Operating voltage: 2.0V~5.5V
* Serial mode for the SC9200A
* Serial/parallel mode for the SC9200B
* Low standby current
* Low total harmonic distortion
* 3.58MHz crystal or ceramic resonator

SELECTION TABLE

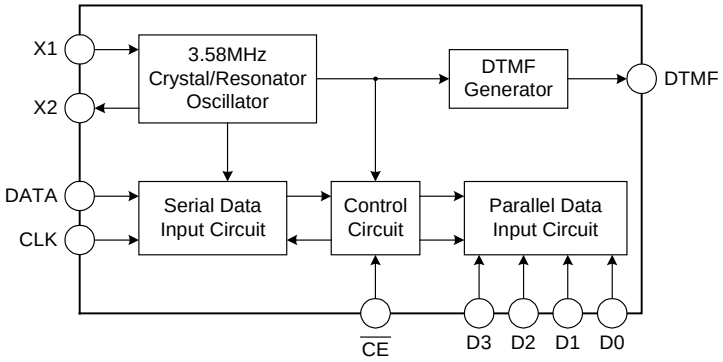
Function / Part No.	Operating Voltage	OSC Frequency	Interface	Package
SC9200A	2V-5.5V	3.58MHz	Serial	8 DIP/SOP
SC9200B	2V-5.5V	3.58MHz	Serial/Parallel	14 DIP/SOP

PIN CONFIGURATIONS





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{SS}	-0.3~6	V
Input Voltage	V_{IN}	V_{SS}-0.3~V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50~125	°C
Operating Temperature	T_{OPR}	-20~75	°C

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
		V_{DD}	Conditions				
Operating Voltage	V_{DD}	--	Serial	1.8	--	5.5	V
			Parallel	2.0			
Operating Current	I_{DD}	2.5V	$\overline{S/P}$ =V_{DD}, D0~D3=V_{SS}, $\overline{CE}$ =V_{SS}, No load	--	240	2500	μA
		5.0V		--	950	3000	
Low Input Voltage	V_{IL}	--	--	V_{SS}	--	0.2V_{DD}	V
High Input Voltage	V_{IH}	--	--	0.8V_{DD}	--	V_{DD}	V
Standby Current	I_{STB}	2.5V	$\overline{S/P}$, $\overline{CE}$ =V_{DD}, No load	--	--	1	μA
		5.0V		--	--	2	
Pull-high Resistance	R_P	2.5V	V_{OL}=0V	120	180	270	kΩ
		5.0V		45	68	100	
DTMF Output Delay Time (Parallel Mode)	t_{DE}	5V	--	--	t_{UP}+6	t_{UP}+8	ms
DTMF Output DC Level	V_{TDC}	2V~5.5V	DTMF Output	0.45V_{DD}	--	0.75V_{DD}	V
DTMF Sink Current	I_{TOL}	2.5V	V_{DTMF}=0.5V	-0.1	--	--	mA
DTMF Output AC Level	V_{TAC}	2.5V	Row group, R_L=5kΩ	0.12	0.15	0.18	Vrms
Column Pre-emphasis	A_{CR}	2.5V	Row group=0dB	1	2	3	dB
DTMF Output Load	R_L	2.5V	t_{HD}≤-23dB	5	--	--	kΩ
Tone Signal Distortion	t_{HD}	2.5V	R_L=5kΩ	--	-30	-23	dB
Clock Input Rate (Serial Mode)	f_{CLK}	--	--	--	100	500	kHz
Oscillator Starting Time (When $\overline{CE}$ is low)	t_{UP}	5.0V	The time from $\overline{CE}$ falling edge to normal oscillator operation	--	--	10	ms
System Frequency	f_{OSC}	--	Crystal=3.5795MHz	3.5759	3.5759	3.5831	MHz

PIN DESCRIPTIONS

Pin NO.	Pin Name	I/O	Internal Connection	Description
1	$\overline{CE}$	I	CMOS IN Pull-high	Chip enable, active low
2	X2	O	Oscillator	The system oscillator consists of an inverter, a bias resistor, and the required load capacitor on chip. The oscillator function can be implemented by Connect a standard 3.579545MHz crystal to the X1 and X2 terminals.
3	X1	I		
4	V_{SS}	--	--	Negative power supply.
5	NC	--	--	No connection.
6~9	D0~D3	I	CMOS IN Pull-high or floating	Data inputs for the parallel mode. When the IC is operating in the serial mode, the data input terminals (D0~D3) are included with a pull-high resistor. When the IC is operating in the parallel mode, these pins become floating.
10	$\overline{S/P}$	I	CMOS IN	Operation mode selection input $\overline{S/P}$ ="H": Parallel mode $\overline{S/P}$ ="L": Serial mode
11	CLK	I	CMOS IN Pull-high or floating	Data synchronous clock input for the serial mode. When the IC is operating in the parallel mode, the input terminal (CLK) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.
12	DATA	I	CMOS IN Pull-high or floating	Data input terminal for the serial mode. When the IC is operating in the parallel mode, the input terminal (DATA) is included with a pull-high resistor. When the IC is operating in the serial mode, this pin becomes floating.
13	DTMF	O	CMOS OUT	Output terminal of the DTMF signal
14	V_{DD}	--	--	Positive power supply, 2.0V~5.5V for normal operation

FUNCTIONAL DESCRIPTION

The SC9200A/B are DTMF generators for μC interfaces. They are controlled by a μC in the serial mode.

1. Serial mode (SC9200A/B)

The SC9200A/B employ a data input, a 5-bit code, and a synchronous clock to transmit a DTMF signal. Every digital of a phone number to be transmitted is selected by a series of inputs that consist of 5-bit data. Of the 5 bits, the D0 (LSB) is the first received bit. The SC9200A/B will latch data on the falling edge of the clock (CLK pin). The relationship between the digital codes and the tone output frequency is shown in Table 1 as for the control timing diagram, refer to Figure 1.

Table 1: Digits vs. input data vs. tone output frequency (serial mode)

Digit	D4	D3	D2	D1	D0	Tone Output Frequency (Hz)
1	0	0	0	0	1	697+1209
2	0	0	0	1	0	697+1336
3	0	0	0	1	1	697+1477
4	0	0	1	0	0	770+1209
5	0	0	1	0	1	770+1336
6	0	0	1	1	0	770+1477
7	0	0	1	1	1	852+1209
8	0	1	0	0	0	852+1336
9	0	1	0	0	1	852+1477
0	0	1	0	1	0	941+1336
*	0	1	0	1	1	941+1209
#	0	1	1	0	0	941+1477
A	0	1	1	0	1	697+1633
B	0	1	1	1	0	770+1633
C	0	1	1	1	1	852+1633
D	0	0	0	0	0	941+1633
--	1	0	0	0	0	697
--	1	0	0	0	1	770
--	1	0	0	1	0	852
--	1	0	0	1	1	941
--	1	0	1	0	0	1209
--	1	0	1	0	1	1336
--	1	0	1	1	0	1477
--	1	0	1	1	1	1633
DTMF OFF	1	1	1	1	1	--

*Notes: The codes not listed in Table 1 are not used D4 is MSB.

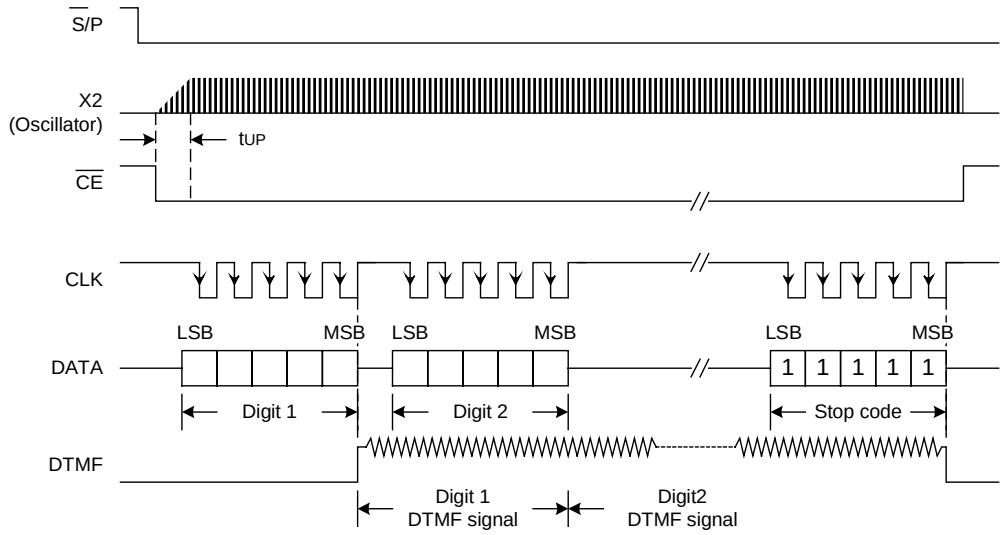


Figure 1

2. Parallel mode (SC9200B)

The SC9200B provides four data inputs D0~D3 to generate their corresponding DTMF signals. The $\overline{S/P}$ has to be connected high to select the parallel operation mode. Then the input data codes should be determined. Finally, the $\overline{CE}$ is connected low to transmit the DTMF signal from the DTMF pin.

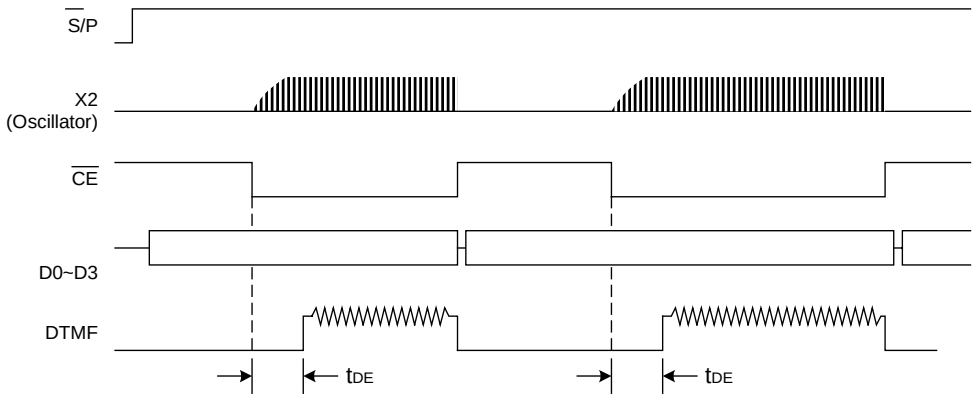
The TDE time (about 6ms) will be delayed from the $\overline{CE}$ falling edge to the DTMF signal output.

The relationship between the digital codes and the tone output frequency is illustrated in Table 2. As for the control timing diagram, see figure 2.

When the system is operating in the parallel mode, D0~D3 are all in the floating state. Thus, these data input pins should not float.

Table 2: Digits vs. input data vs. tone output frequency (parallel mode)

Digit	D3	D2	D1	D0	Tone Output Frequency
1	0	0	0	1	697+1209
2	0	0	1	0	697+1336
3	0	0	1	1	697+1477
4	0	1	0	0	770+1209
5	0	1	0	1	770+1336
6	0	1	1	0	770+1477
7	0	1	1	1	852+1209
8	1	0	0	0	852+1336
9	1	0	0	1	852+1477
0	1	0	1	0	941+1336
*	1	0	1	1	941+1209
#	1	1	0	0	941+1477
A	1	1	0	1	697+1633
B	1	1	1	0	770+1633
C	1	1	1	1	852+1633
D	0	0	0	0	941+1633



*Note: The data (D0~D3) should be ready before the $\overline{CE}$ becomes low.

Figure 2

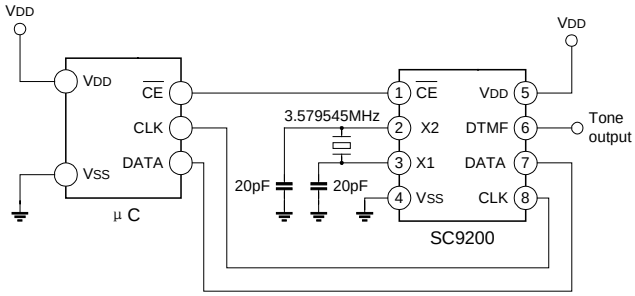
Tone frequency

Output Frequency (Hz)		%Error
Specified	Actual	
697	699	+0.29%
770	766	-0.52%
852	847	-0.59%
941	948	+0.74%
1209	1215	+0.50%
1336	1332	-0.30%
1477	1472	-0.34%

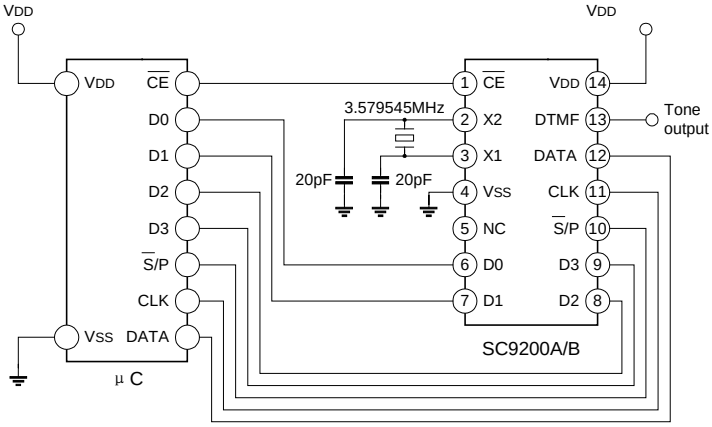
% Error does not contain the crystal frequency drift

APPLICATION CIRCUIT

Serial mode

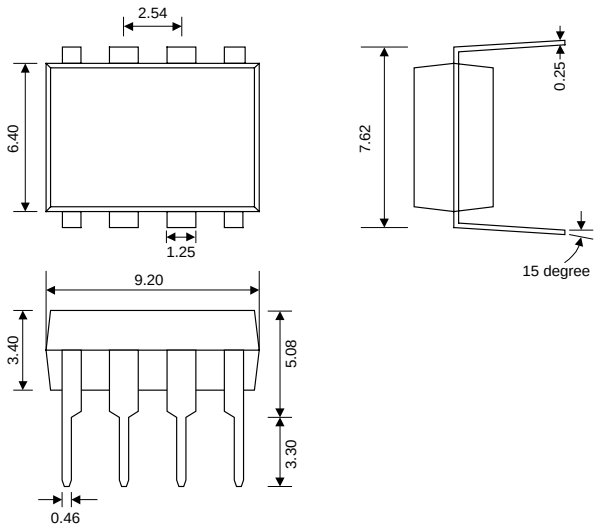


Serial/parallel mode



PACKAGE OUTLINE

DIP-8-300-2.54 UNIT: mm



DIP-14-300-2.54 UNIT:mm